IN THE SPECIFICATION:

Please replace the first paragraph of page 38 with the following new paragraph:

Fig; 9(E) shows another cross section of a TFT circuit fabricated in the present example. This is a cross section taken along the phantom line A-B of Fig. 9(D) through an N-channel TFT. As can be seen from this figure, crystallized doped regions 912, 913' and an intervening element-isolating region (a separation semiconductor) 914 are on the same plane and, therefore, the gate electrode [[917]] 907 is flat. A wiring layer 917' which is in contact with the doped region 913' and with a gate electrode 907 has steps only in the locations of the contact holes and in the location of the interlayer insulator. Neither steps of island semiconductor regions as in Example 1 nor steps of thick insulating film for isolation of elements as in Example 5 exist. This is advantageous for manufacturing integrated circuits at a higher density with a high production yield. In the device shown in Fig . 9(D), the transistors are separated from each other by the separation semiconductor 914 provided between the crystalline semiconductor regions 904.